

FIGURE 1

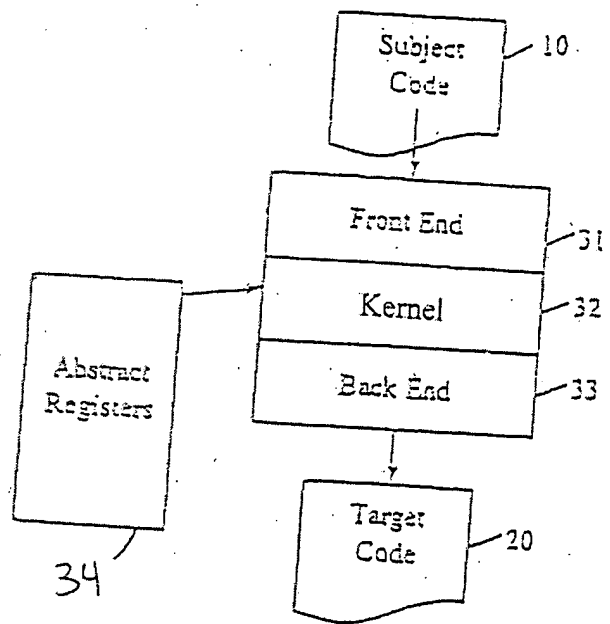


FIGURE 2

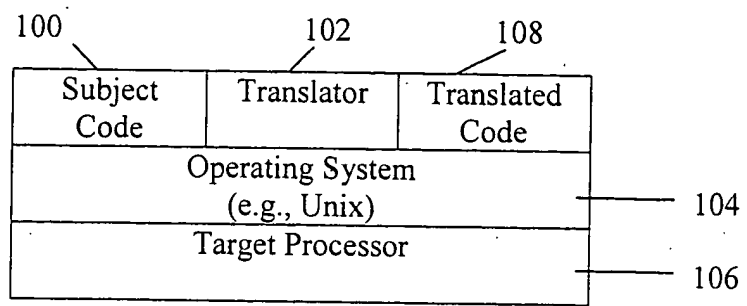


Figure 3

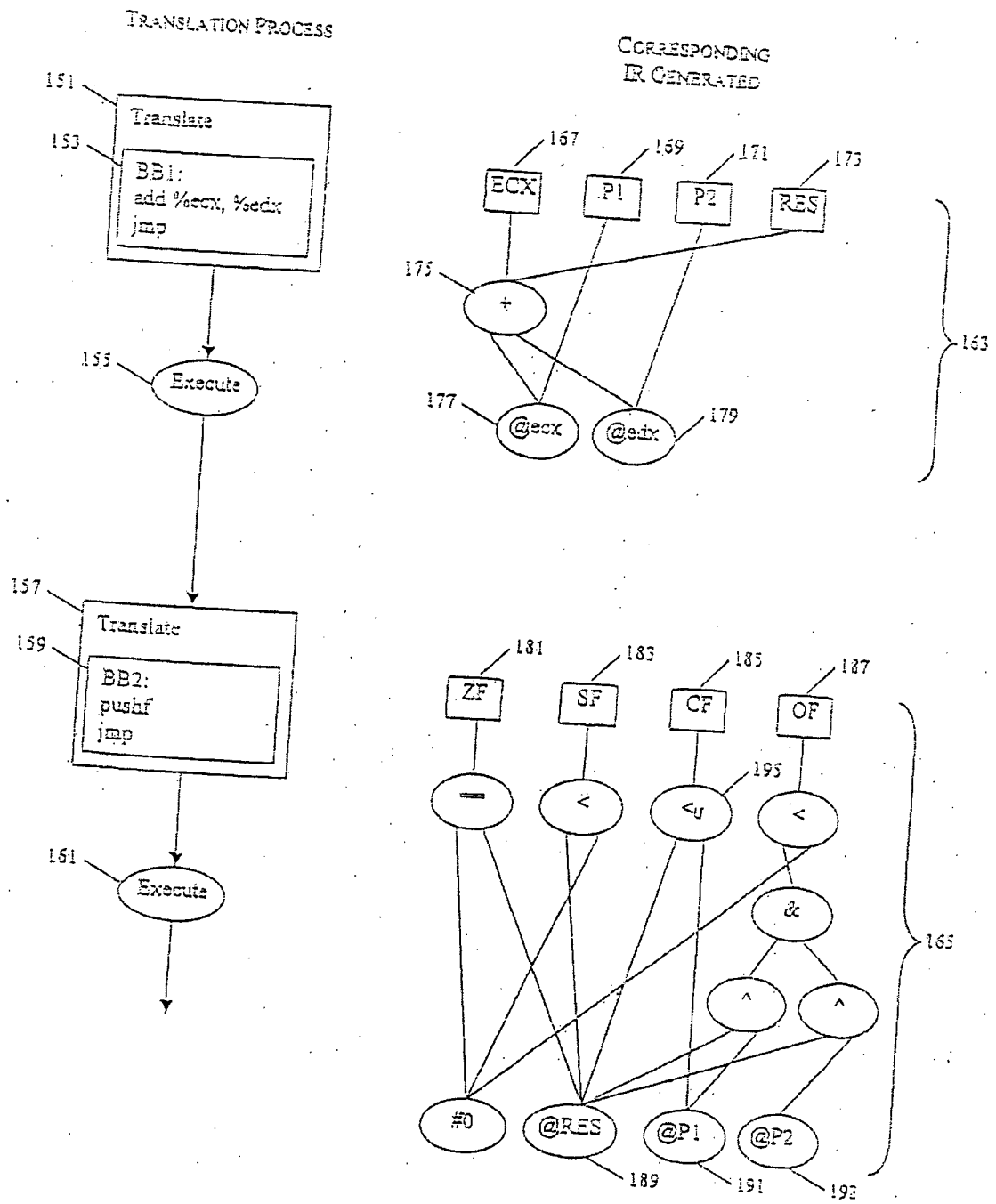


FIGURE 4

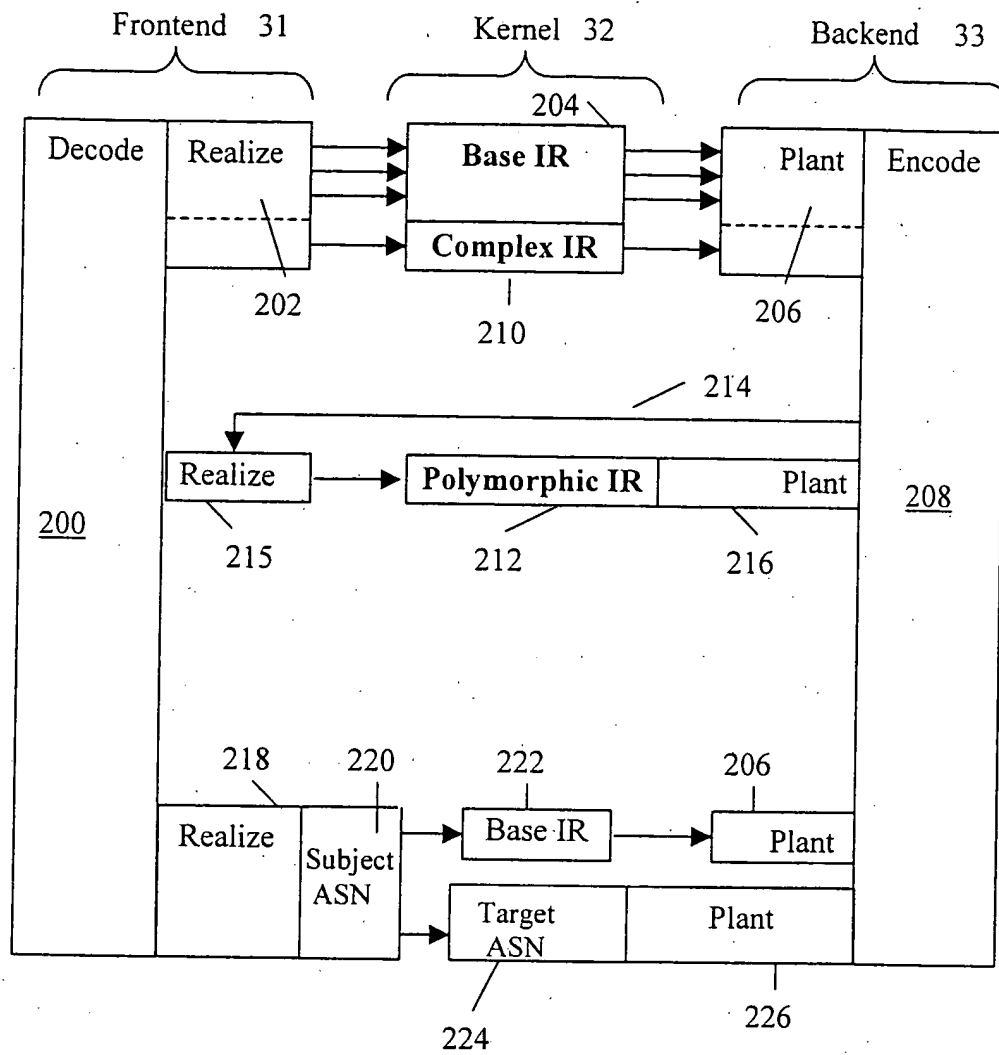
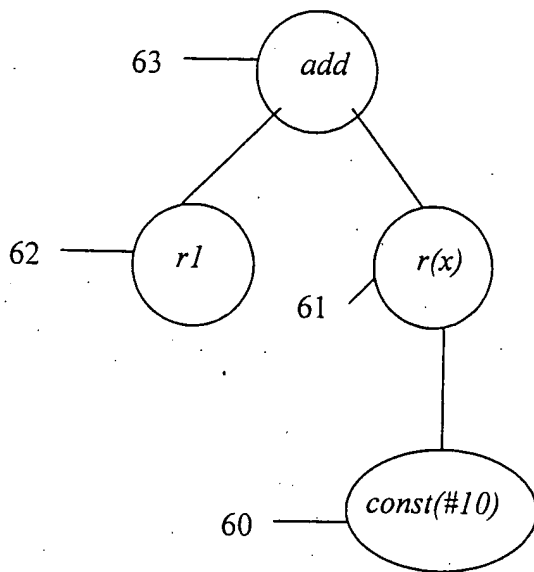


FIG. 5

Instruction: `addi r1,#10`

Base Node Representation



Complex Node Representation

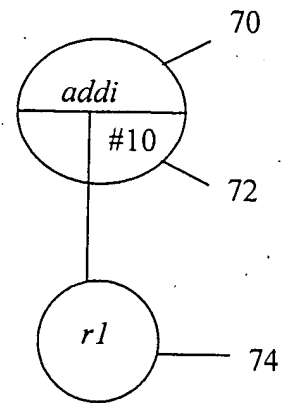


FIG. 6

FIG. 7

MIPS-MIPS ACCELERATOR

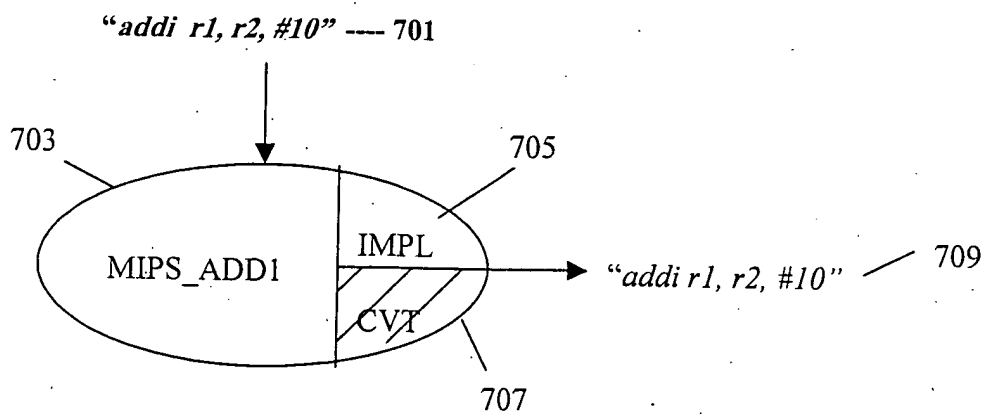


FIG. 8

MIPS-X86 TRANSLATOR

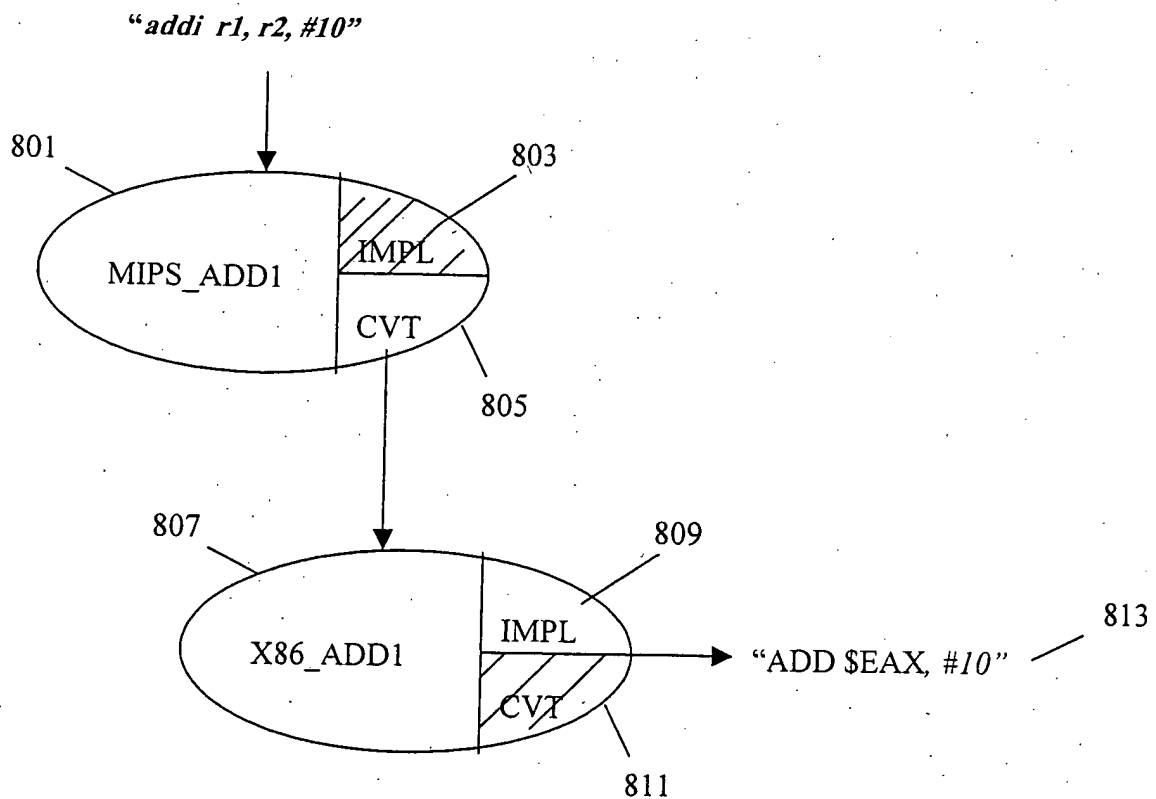
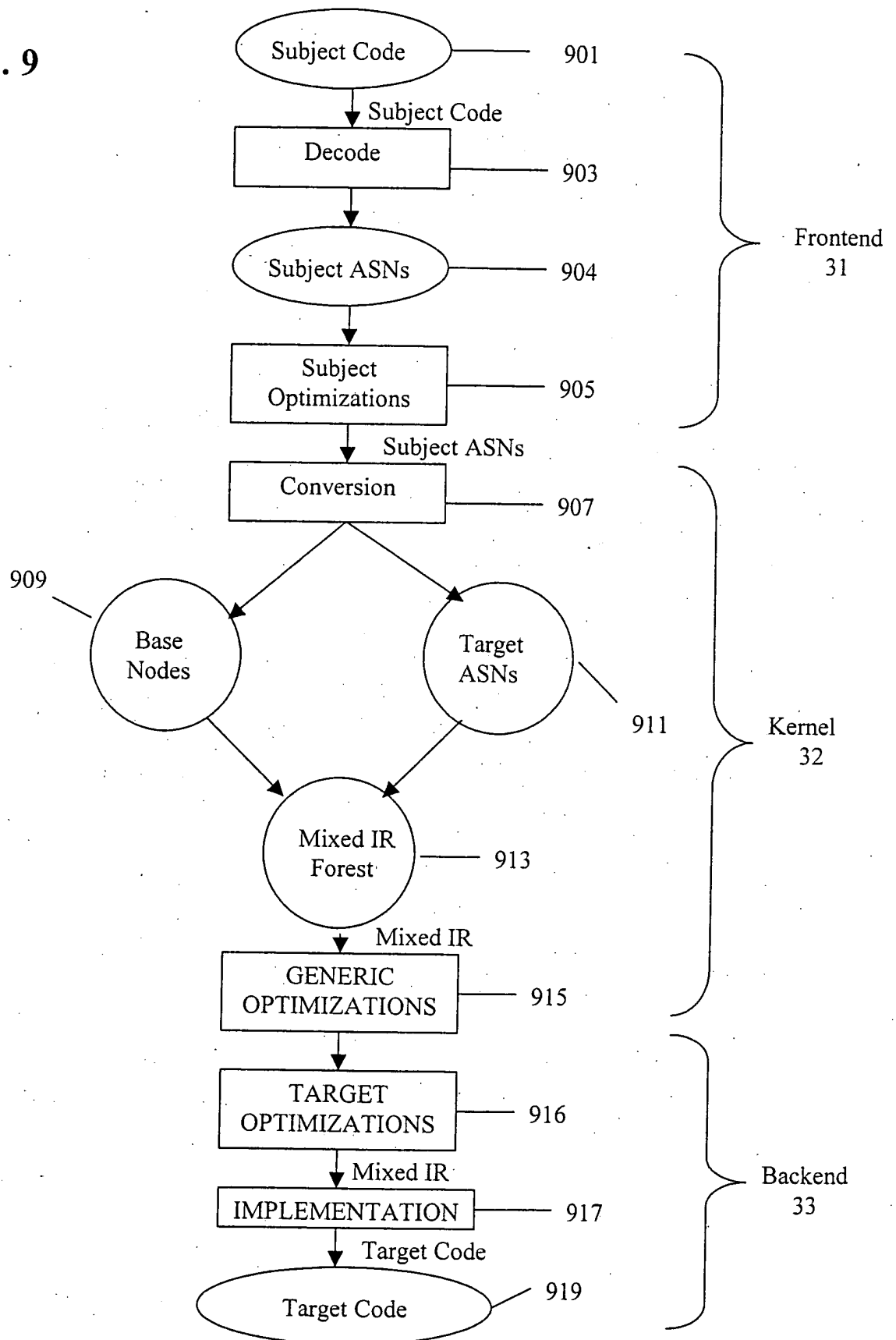


FIG. 9



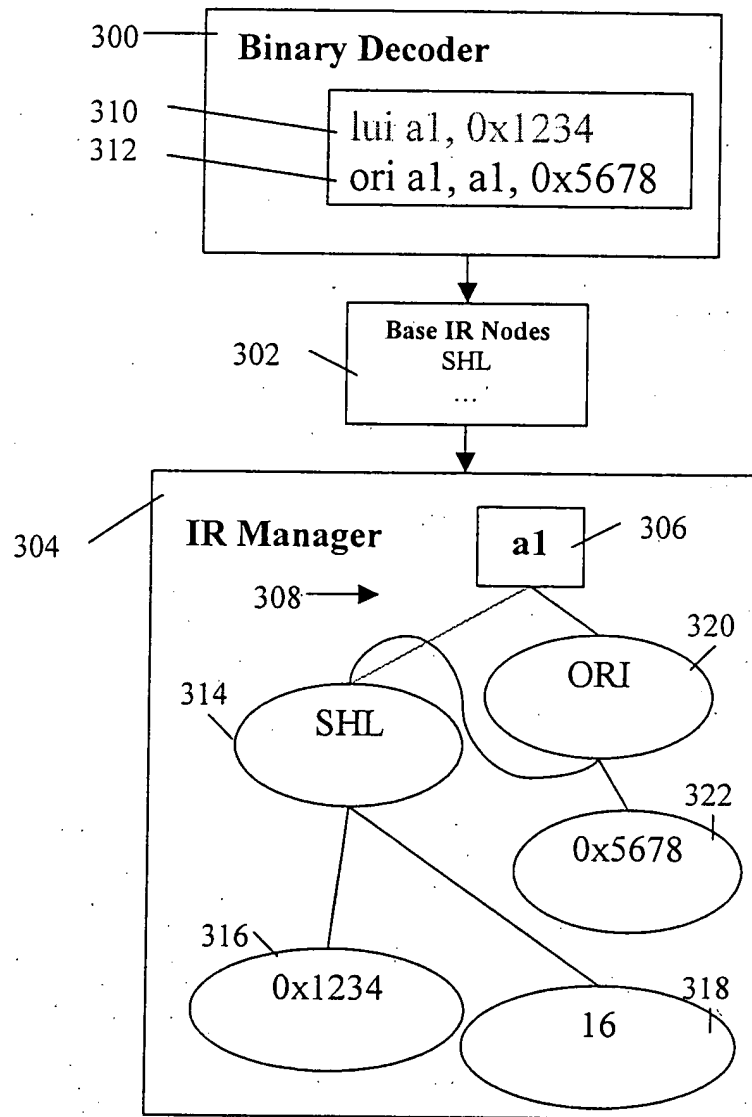


FIG. 10

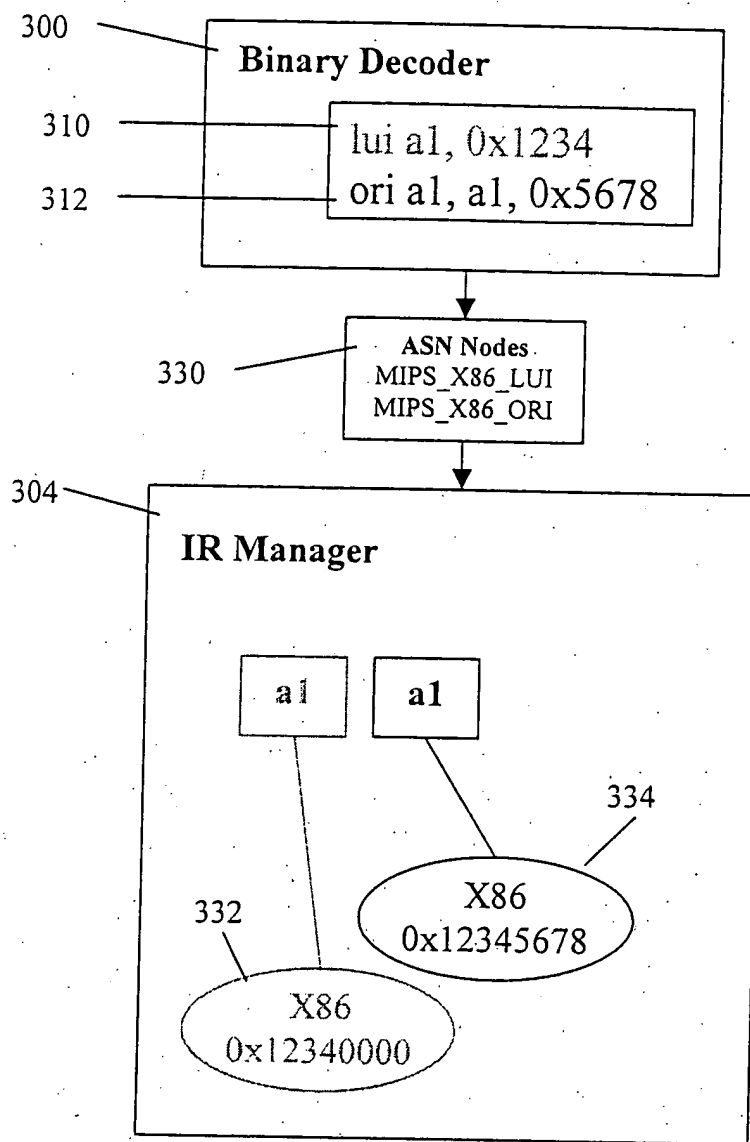


FIG. 11

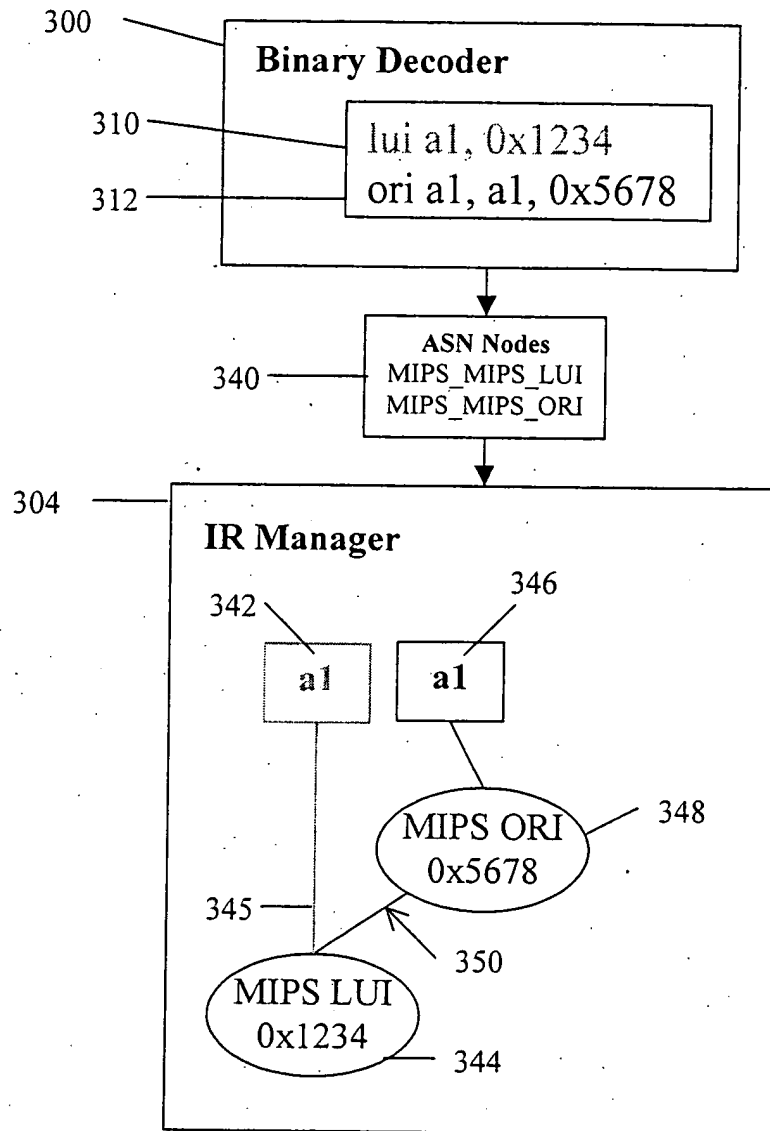


FIG. 12